SIGMA 5 THROUGH 9
REMOVABLE DISK STORAGE TEST
PROGRAM NO. 705534B

901612C
Price: $.50

DIAGNOSTIC PROGRAM MANUAL

SIGMA 5 THROUGH 9 REMOVABLE DISK STORAGE TEST

PROGRAM NO. 705534C

Specifications and procedures contained herein are subject to change without notice.

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SUBJECT MODEL -- Removable Disk Controller, Model number 7240, Removable Disk Storage Units, Model numbers 7242, 7246

REQUIRED EQUIPMENT -- Minimum Memory Size: 16K; Input Device: Card Reader, Paper Tape Reader or Magnetic Tape Unit; Output Device: Keyboard Printer or Line Printer

PROGRAM PREREQUISITES

None

GENERAL OPERATING PROCEDURES

General operating procedures of the XDS Sigma 5 through 9 Diagnostic Program Monitor (DPM), Manual No. 901649, apply to this program.

DIRECTIVES - directives are entered after a "!" is typed out

Name	Format	Parameter			
		ID	Definition	Value Range	Standard Value (default)
		Program Directives - Environmental Directives			
System Environment	SYST, D1, D2, H3, H4, H5, H6 ,H7 . . . ,H17,H18	D1 D2 H3 H4 H5 H6 : H17 H18	Controller model number Revision number Storage Unit Device Address (1st) Available cylinders (1st) Storage Unit Device Address (2nd) Available cylinders (2nd) Same as H3, H4 except for 8th Storage Unit	7240 0 80 ~ 1FFF 00XY00ZW 80 ~ 1FFF 00XY00ZW XY = 1st cylinder ZW = last cylinder	
		Program Directives - Testing Directives			
Comprehensive Test (all functional tests, 1 70, and random exerciser Test)	TST0, D1, D2	D1 D2	Number of ordered sequences executed by random exerciser Number of retries	0 ~ 99999999 0 ~ 99999999	5000 (D1 = 0) 0
Functional Test	TST1 [, D1 [, D2]]	D1 D2	The first subtest to be executed Last subtest to be executed	0 (all subtests) ~ 70 1	0 D1
Random Exerciser Test	TST2, D1, D2	D1 D2	Number of cycles to be performed Number of retries before next cycle	D1 > 0 D2 ≥ 0	
Utility Test	TST3, D1, D2, D3, H4		D1 - Utility Test selection D2 - Function selection or serial number D3 - Retry count; not used if D1 = 3 D1 = 1 Surface Test D2 = 0 Write and then read all sectors D2 = 1 Write all sectors D2 = 2 Read all sectors D2 = 3 Read all sectors (no data check) D2 = 4 Checkwrite all sectors D2 = 5 Write and then checkwrite all sectors D1 = 2 Header Test D2 = 0 Write and then read all headers D2 = 1 Write all headers D2 = 2 Read all headers D2 = 3 Read all headers (no data check) D1 = 3 Disk Initialization D2 = Pack serial Number D3 = 0 - Not used H4 = Date = 00MMDDYY D1 = 4 Flaw A Track D2 = Alternate Cylinder Address D3 = Alternate Head ADR	 200 ~ 202 0 - 19	
		Program Directives - Optional Directives			
Pattern selection (for Utility Test)	DATA, D1, H2, H3	D1 H2 H3	= 0, Fixed Pattern = 1, Incremental Pattern = 2, Random Pattern = 3, Current Seek Address Pattern seed (for D1 = 0, 1, 2) Incrementing constant (for D = 1)	0 ~ 3 00000000 ~ FFFFFFFF	
Usable surface area limitation	SEEK, D1, D2, D3, D4	D1 D2 D3 D4	Starting cylinder address Starting head address Starting sector address Additional sectors to be used after starting address D1, D2, D3	0 ~ 202 0 ~ 19 0 ~ 5 (0 ~ 81)	
Limitation of Error printouts	LIMT, D1, D2	D1 D2	= 1 Limit Compare error printouts/sector to D2 Maximum number of printouts (No limit if D2 = 0)	1 D2 ≥ 0	
I/O buffer area definition	MEM [, H1, H2]	H1 H2	First location of I/O buffer area Last location of I/O buffer area	Obtainable by typing in MEM/	Area between Diag. Prog. & DPM
I/O Reset	RSET	0			Not available

Note: Parameter of any directive beginning with a D means decimal, with an H means hexadecimal

START PROCEDURE

1. Sense Switch Options, Monitor Directive Options, and Environmental Directives - Refer to XDS DPM Manual No. 901649
2. Test Strategy Selection

	Comprehensive Test	Functional Test	Random Exerciser Test	Utility Test
Recommended Application	Normal Usage	Solid Failure Detection and Specific Problem Analysis	Intermittent Failure Detection	Surface Test
Test Directive	TST0	TST1	TST2	TST3
Prerequisite	None	None	TST1	TST1
Optional Directives	SEEK, LIMT, MEM	SEEK, LIMT, MEM	SEEK, LIMT, MEM	SEEK, LIMT, MEM, DATA
Subtests	All functional subtests (1 ~ 70) and random exerciser test	70 subtests (see error messages for the test types)	1. Exerciser Initiation: Random data written on entire surface 2. Random Selection of: a. Device b. Order Sequences c. Buffer Areas d. Buffer Length e. Data	WRITE only READ only (Verify data) READ only (No data verification) READ header CHECKWRITE WRITE/READ TEST WRITE header
Error Message Format	1. ERROR NO. DDDD LOC XXXX 2. Self-explanatory	ERROR NO. DDDD LOC XXXX	Self-explanatory	Self-explanatory

3. Procedure 2 of Restart Procedure of XDS DPM 901649 should normally be used to clear a wait from a watchdog timer trap

PROGRAM TEST DESCRIPTION

Test descriptions of each functional test are included at the beginning of each subtest error number in the Functional Subtest and Related Error Message Section.

ORDER CODES

X'00' STOP
X'01' WRITE
X'02' READ 2 (Report any transmission error at "count done")
X'03' SEEK
X'04' SENSE
X'05' CHECKWRITE
X'12' READ 1 (Terminate data transfer and report any transmission error at end of current sector if error is encountered)
X'13' SELECT TEST MODE
X'80' STOP AND INTERRUPT (at location X'5C')
X'09' HEADER WRITE
X'0A' HEADER READ
X'33' RESTORE CARRIAGE
X'23' RELEASE

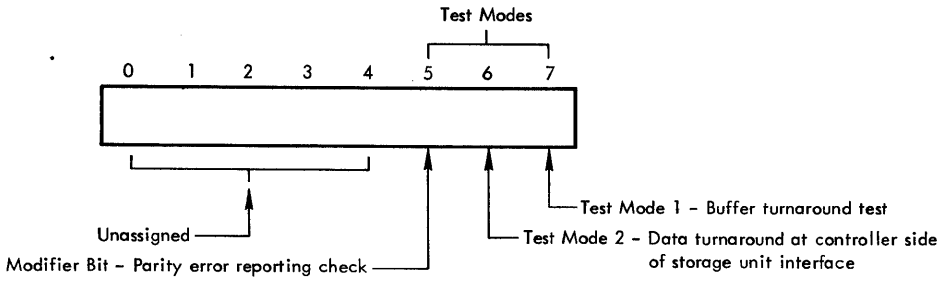
TDV STATUS

	BITS							
MODEL	0	1	2	3	4	5	6	7
REM DISK	Data Overrun	Flaw Mark	Sector Unavailable	Unassigned	Header Verification Error	Head On Cylinder	Seek Timeout Error	Header Parity Error

AIO STATUS

	BITS							
MODEL	0	1	2	3	4	5	6	7
REM DISK	Data Overrun	← UNASSIGNED →				Head On Cylinder	Seek Timeout Error	Unassigned

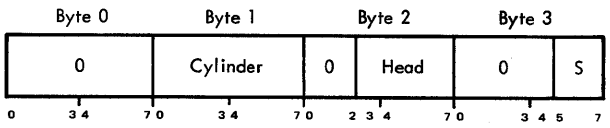
TEST MODE DATA BYTE



ADDRESSING FORMAT

1. The format of the four byte sent to the Disk Pack by a SEEK order is:

Model 7240

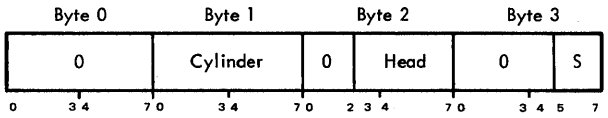


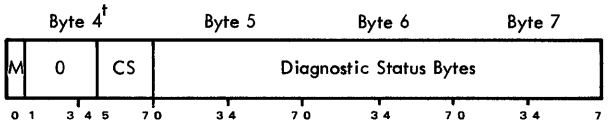
where S signifies sector number.

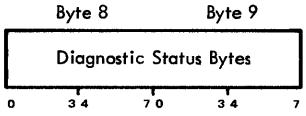
2. The format of the bytes received on a SENSE order is:

SENSE (X'04')

The Sense order causes the controller to transmit up to 10 bytes of information to the IOP, as follows:







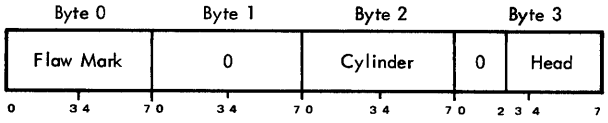
where
- S signifies sector number
- M signifies modifier bit
- CS signifies current sector number

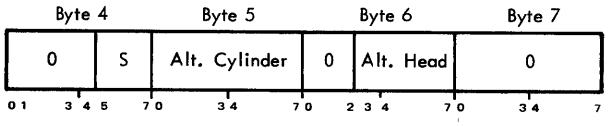
†Three bits of byte 4 indicate current sector number, but if the most significant bit (M) is a 1, the arm was in motion at time of sense and current sector number is meaningless. If the head number is nonexistent, (M) will also be a 1.

3. The format of the 8 bytes sent to the Disk Pack by a WRITE header order is:

HEADER WRITE (X'09')

The Header Write order causes the controller to consider all subsequent data bytes as header information. Each header requires the following bytes:





Sense Status Bytes 8 and 9

Byte No.	Bit No.	Function
8	0	Data parity error
	1	Check-Write error
	2	Sector verification error
	3	Head verification error
	4	Cylinder verification error
	5	Sector address not zero at start of header write operation
	6	Difference select sent to device
	7	Sector select sent to device
9	0	Control select sent to device
	1	Head select sent to device
	2	Cylinder select sent to device
	3	Seek forward set
	4	Read gate sent to device
	5	Write and erase gate sent to device
	6	Read cylinder select sent to device
	7	Not used

Note: Bytes 8 and 9 are used by diagnostic programs.

FUNCTIONAL SUBTESTS AND RELATED ERROR MESSAGES

FAULT INDEX DESCRIPTION - FUNCTIONAL SUBTESTS

The fault index contains a brief description of each functional subtest and a list of associated error numbers with a brief description of each error. The subtests and error numbers are arranged in ascending sequence. The description of subtest NN is numbered NN00. The first two digits of the error number correspond to the associated subtest; the last two numbers correspond to the individual errors within the subtest.

System error numbers

8500 Controller did not return to Ready condition after Test Mode order.
8501 Controller not in Test Mode after Test Mode order. TDV CC = 0.
8502 Controller in Test Mode after resetting Test Mode. TDV CC = 4.
8510 Controller did not return to Ready condition after Restore order.
8511 Device not on cylinder after a Restore order.

TST1, 01 AIO, HIO, TIO, TDV instruction recognition.

0110 AIO Condition Code error. No interrupt recognition expected.
0111 HIO Condition Code or Status error. See print-out.
0112 TIO Condition Code or Status error. See print-out. Preceding HIO did not reset Status.
0113 TDV Condition Code error. See print-out.

TST1, 02 SIO Invalid Order Test

0210 SIO for Invalid order not accepted. See print-out.
0211 Controller not ready after Invalid order (00 or F8). Order output and order input phases must be executed.
0212 Status error after Invalid order. UE expected.
0213 Byte count was changed during execution of Invalid order. Data phase not required.

TST1, 03 Test Mode Selection Test. A TDV instruction is used to verify setting and resetting of Test Mode.

0301 Test Mode byte = X'FF'.
0302 Test Mode byte = X'01'.
0303 Test Mode byte = X'02'.
0310 TDV CC2 reset. Device controller not in Test Mode.
0311 Output buffer changed during Test Mode order (Select). Data in phase not expected.
0312 TDV CC2 set. Device controller remains in Test Mode. CC2 = 0 expected.
0313 Output buffer contains ones after Test Mode order (Reset).
0315 TIO CC1 or CC2 set. Controller not ready after Test Mode order.
0316 TDV, TIO Status error or byte count error. See preceding print-out. Operation: Order out (X'13'), data out (1 byte), order in.
0321, 0322, 0323 TST1, 3 Data byte of FF, 01, and 02 was used during data output phase. See preceding print-out.

TST1, 04 Interrupt generation and HIO, AIO Instruction Test. The following orders will be issued: X'00', X'13' (data byte = 01), X'1' (data byte = 00) in order to set Interrupt Pending due to IUE, ICE and IZC respectively. Each order will be repeated once to allow resetting of IP with an HIO and an AIO instruction.

0410 TIO Status error during TST1, 4 after SIO. IP must be set and controller and device must be ready. IUE, ICE, and IZC flags are used.
0411 HIO did not reset IP. No reset generated.
0412 AIO Status error during TST1, 4. Preceeding SIO resulted in IP.
0413 AIO did not reset IP. No reset generated.
0421, 0422, 0423 TST1, 4 IOP flags for IUE, ICE, and IZC used respectively. See print-out.

TST1, 05 IO Interrupt Test. A Test Mode order with ICE flag will be issued and tests will be performed to verify that the program is only interrupted if the IO Interrupt is armed and enabled.

0510 TIO Status error during TST1, 5 after SIO. IP must be set. IO Interrupt is disarmed/disabled. Program should not be interrupted.
0511 Program was interrupted while IO Interrupt was disarmed/disabled.
0512 Program was interrupted while IO Interrupt was armed/disabled.
0513 Program was not interrupted while IO Interrupt was armed/enabled.

TST1, 06 Command Chaining Test. Two Test Mode orders will be Command Chained. Command Chaining will be tested. Invalid order Command Chained to a Test Mode order should not result in Command Chaining.

0610 TIO Status error during TST1, 6 after Command Chaining or Command Chaining not performed. See preceding printout.
0611 TIO Status error during TST1, 6. Status error or Command Chaining not inhibited by UE from Invalid order.

TST1, 07 FAM Write/Read Byte Count Test. Write and Read orders with byte counts varying sequentially from 1 to 16 are issued in Test Mode 1. Zero byte count expected.

0710 Controller not ready after Write order in TM1.
0711 Controller not ready after Read order in TM1.
0712 Byte count not equal to zero after Write order in TM1.
0713 Byte count not equal to zero after Read order in TM1.

TST1, 08 FAM Write/Read Data Test. Write Command-Chain Read orders will be issued with varying data pattern. The Read data will be compared to the Write data. During the 2nd part of the test 4 Write/CC/Read orders with counts of 13 will be issued to test the byte alignment logic.

0810 Controller not ready after Write/CC/Read order in TM1.
0811 Compare errors during TST1, 8. Output buffer: IOBF1, Input buffer: IOBUF.
0812 Controller not ready after Write/CC/Read (BC = 13) Test Mode 1.
0813-0816 Read Data compare error following Write/CC/Read (BC = 13)
If last digit is 3, data started on word boundary
If last digit is 4, data started at byte 1
If last digit is 5, data started at byte 2
If last digit is 6, data started at byte 3

TST1, 09 Test Mode 2 - Seek Order Byte Count Test. Seek orders with byte counts of 3, 4, 5 are issued to the controller and the status response is tested.

0910 Controller not ready after Seek order in Test Mode 2.
0911 Status error after Seek order in Test Mode 2. Expected: IL, UE, zero byte count, on-cylinder. See printout.
0912 Status error after Seek order in Test Mode 2. Expected: Not IL, zero byte count, on cylinder. See printout.
0913 Status error after Seek order in Test Mode 2. Expected: IL, byte count = 1, on-cylinder. See printout.
0914 Output buffer (:IOBF1) altered during Seek in TM2.

TST1, 10 Test Mode 2 - Seek Order Interrupt Address Test. Seek orders will be to device 0 through 7 in sequence and the address returned with the AIO Status will be verified. Change above mask from X'04000000' to X'0C000000' if Device Interrupt Engineering Order is available.

1010 Status error after Seek order with Interrupt Modifier bit. Expected: IP, zero byte count, on cylinder. See printout.
1011 AIO Status error after Seek order with Interrupt Modifier bit. IP set prior to AIO. Expected: Address verification. See printout.
1012 Preceding AIO did not clear Seek complete interrupt (TIO/IP=0).

TST1, 13 Test Mode 2 - Sense Order Byte Count Test. Sense orders with byte counts of 1 through 11 are issued to the controller and the Status Response is tested.

1310 Controller not ready after Sense order in Test Mode 2.

TST1, 13 (Continued)

1311 Status error after Sense order in Test Mode 2. No unusual status expected. See print-out.
1312 Byte count not equal to zero after a Sense order with a byte count ≤ 10. See print-out.
1314 First 8 bytes of input buffer (IOBF1) not changed during Sense order. Data input expected.

TST1, 15 Test Mode 2 - Seek Tag Line Test. See/Command Chain/ Sense orders are executed and the Tag Line information in byte 8 of the Sense data is verified.

1510 Controller not ready after Seek/CC/Sense order in Test Mode 2.
1511 Status error after Sense order or Command Chaining not performed. See print-out
1512 Seek Tag Line error or Sense order not functioning properly. Sense buffer: IOBF1. See print-out.

TST1, 16 Test Mode 2 - Head and Sector Address Test. Seek/CC/ Sense orders are issued sequentially varying the Device Address from 0 - 7. Sense data is verified. Sense orders are issued sequentially to all devices to insure that the addresses are not changed. The same sequence is repeated with the Device Address varied from 7 - 0. The complement of the data pattern in pass 1 is used in Pass 2. A unique pattern is used for each device.

1610 Controller not ready after Seek/CC/Sense order in Test Mode 2.
1611 Controller not ready after Sense order in Test Mode 2.
1620-1627 Head and Sector Address obtained during Sense not equal to original data. Last digit of error number indicates Device Address used. Address sequence 0 - 7. Order sequence: Seek/ CC/Sense.
1630-1637 Head and Sector Address obtained during Sense not equal to original data. Check addressing of Head and Sector FAM. Last digit of error number indicates Device Address used.
1640-1647 Same as 1620-1627. Address sequence 7 - 0.
1650-1657 Same as 1630-1637.

TST1, 17 Test Mode 2 - Head and Sector Address Validy Test. Seek and Sense are issued 203 times varying the Sector Address from 0-7 and the Head Address from 0-25. Sector unavailable will be tested for Sector Address > 5 and Head Address > 19. The combined Sector and Head Address which is returned as Cylinder Address during Seek will be verified.

1710 Controller not ready after Seek order in Test Mode 2.
1711 Status error after Seek order in Test Mode 2 with illegal sector Address (7). UE, sector unavailable, on cylinder expected.
1712 See 1711. Illegal Head Address was issued during Seek.
1713 Status error after Seek order in Test Mode 2. Legal Head and Sector Address were used. See print-out.
1714 Controller not ready after Sense order in Test Mode 2.
1715 Seek/Sense compare error. The Head/Sector Address was not returned correctly as the Cylinder Address. See print-out.

TST1, 19 Test Mode 2 - Cylinder Difference Logic Test. Seek and Sense orders are issued systematically varying the Cylinder and Head/Sector Address. 5 passes will be performed:

1. Cyl and Hd/Sect = 0 - 202.
2. Cyl = 0 - 202, Hd/Sect = 0
3. Cyl = 0, Hd/Sect = 0 - 202
4. Cyl = 202 - 0, Hd/Sect = 0
5. Cyl = 0, Hd/Sect = 202 - 0

1910 Controller not ready after Seek order in Test Mode 2.
1911 Controller not ready after Sense order (Byte count = 10) in Test Mode 2.
1912 The difference between Head/Sector and the Cylinder Address returned in byte 7 of the Sense order is not correct. See print-out.
1913 Controller not ready after the 2nd Seek order in Test Mode 2. Two Seek orders are required to obtain the correct difference in byte 7 of the Sense data.

TST1, 20 Test Mode 2 - Illegal Cylinder Address Test. Seek orders are issued with illegal Cylinder Address (203 - 255) and the Status Response is verified.

2010 Controller not ready after Sense order in Test Mode 2.
2011 Status error after Seek order in Test Mode 2 with Illegal Cylinder Address (203 - 255). UE, sector unavailable, on cylinder expected.

TST1, 23 Test Mode 2 - Restore Order Test. A Seek/CC/Restore and Sense order sequence is sequentially issued to all devices (0 - 7). The test verifies the status after the Restore orders and verifies with a Sense order (Byte count = 10) that the Head and Sector Address in the FAM are cleared to zero and that the Restore order generated the correct Tag Lines.

2310 Controller not ready after Seek/CC/Restore orders in Test Mode 2.
2311 Status error after Restore order in Test Mode 2. Not UE, byte count = 1 (no changes). See print-out.
2312 Controller not ready after Sense order in Test Mode 2.
2313 Bytes 2 (Head) and 3 (Sector) of Sense data not 0. Preceding Restore order did not clear controller registers (FAM).
2314 Restore Tag Line error. Sense buffer: IOBF1. See print-out.

TST1, 24 Test Mode 2 - Release Order Test. A Release order and a Sense order is issued. The test verifies the status after the Release and verifies with a Sense order (Byte count = 10) that the Restore order generated the correct Tag Lines.

2410 Controller not ready after Restore order in Test Mode 2.
2411 Status error after Restore order in Test Mode 2. Not UE, byte count = 1 (No change) expected. See print-out.
2412 Controller not ready after Sense order in Test Mode 2.
2413 Release Tag Line error. Sense buffer: IOBF1. See print-out.

TST1, 25 Test Mode 2 - Read Order Tag Line and Data Test. Read orders X'02' and X'12' are issued in sequence. The status and byte count are verified. The Read data is compared to the expected information. A Sense order verifies that the Tag Lines are correctly generated for a Read order.

2510 Controller not ready after Read order (02) in Test Mode 2.
2511 See 2510. Read order (12).
2512 Status error after Read order in Test Mode 2. Not UE, not IL, not TE, byte count = 0 expected. See print-out.
2513 See 2512. Read order (12).
2514 Data compare error in Test Mode 2; Read order (02). See print-out.
2515 See 2514. Read order (12).
2516 Controller not ready after Sense order in Test Mode 2.
2517 Read (02) Tag Line error. Sense buffer: IOBF1. See print-out.
2518 See 2517. Read order (12).
2519 Status error in diagnostic Sense byte (byte 8 of Sense data) defines Read error.
2520 See 2519. Read order (12).

TST1, 26 Test Mode 2 - Read Order Incorrect Length Test. Read orders are issued with byte count sequentially varied from 1008 to 1025 (not 1024). The status will be verified. For byte counts < 1024 the test verifies that the controller terminates data-in at the correct byte count.

2610 Controller not ready after Read order (02) in Test Mode 2.
2611 Remaining byte count after Read order with incorrect length not zero. See print-out.
2612 Status error after Read order in Test Mode 2. IL expected. See print-out.
2613 Data compare error in Test Mode 2; Read order (02). For byte count < 1024 the remaining bytes in input buffer must be zero.

TST1, 27 Test Mode 2 - Read Order/Head and Sector Incrementation Test. Seek/CC/Read and Sense order sequences are issued with a Read byte count of 1024. Sector and Head Address incrementation is verified.

TST1, 27 (Continued)

2710 Controller not ready after Seek/CC/Read (02) orders in Test Mode 2.
2711 Status error after Seek/CC/Read in Test Mode. No abnormal status expected. See print-out.
2712 Controller not ready after Sense order in Test Mode 2.
2713 Address received during Sense not expected. Head or Sector Address may not increment properly. See print-out.

TST1, 28 Test Mode 2 - Read Order Cylinder Boundary Test. A Read order with a byte count of 1025 is issued starting at Head 19, Sector 5. Read operation will terminate after 1 sector and sector unavailable will be reported.

2810 Controller not ready after Seek/CC/Read (02) orders in Test Mode 2.
2811 Status error after Read order (Seek Address = Head 19. Sector 5, byte count = 1025). UE, sector unavailable, byte count = 1 expected: See print-out.

TST1, 29 Test Mode 2 - Header Read Order Test. Seek/CC/Header Read orders sequences are issued with Header Read byte count of 8. The status and byte count are verified. The Header Read data is compared to the expected information. A Sense order verifies that the Tag Lines are correctly generated and that the Head and Sector Address are incremented correctly.

2910 Controller not ready after Seek/CC/Header-Read orders in Test Mode 2.
2911 Status error after Header Read order. No abnormal status expected. See print-out.
2912 Header data compare error in Test Mode 2. See print-out.
2913 Controller not ready after Sense order in Test Mode 2. See print-out.
2914 Header Read Tag Line error. Sense buffer: IOBUF. See print-out.
2915 Status error in diagnostic Sense byte (Byte 8 of Sense data) defines Header Read error.
2916 Address received during Sense not expected. Head or Sector Address may not increment properly. See print-out.

TST1, 30 Test Mode 2 - 120 Sector Header Read Test. A Seek/CC/Header Read order with a Header Read byte count of 960 is issued. The Header data is verified. No data error indicates that the Head and Sector Incrementation Logic performs correctly.

3010 Controller not ready after Header Read order in Test Mode 2.
3011 Byte count not zero after Header Read order (960 bytes).
3012 Status error after Header Read order. No abnormal status expected.
3013 Header data compare error in Test Mode 2. See print-out.

TST1, 31 Test Mode 2 - Header Read Byte Count Test. Header Read orders with byte counts of 7 and 9 are issued to the controller and the Status Response is tested.

3110 Controller not ready after Header Read order in Test Mode 2.
3111 Status error after Header Read order (byte count 7). Expected: IL, no UE, byte count = 0. See print-out.
3112 See 3111. Header Read order byte count = 9.

TST1, 32 Test Mode 2 - Header Read Order Cylinder Boundary Test. A Header Read order with a byte count of 9 is issued starting at Head 19 Sector 5. Read operation will terminate after one sector and sector unavailable will be reported.

3210 Controller not ready after Header Read order in Test Mode 2.
3211 Status error after Header Read order (Seek address = Head 19, Sector 5, byte count = 9). UE, sector unavailable, byte count = 1 expected.

TST1, 35 Test Mode 2 - Header Write Order Test. Seek/CC/Header Write order sequences are issued with Header Write byte counts of 48. The Header data consists of a X'A5A5A5A5' pattern. The status and byte count are verified. A Sense order verifies that the Tag Lines are correctly generated and that the Head and Sector Address increment correctly.

3510 Controller not ready after Seek/CC/Header-Write orders in Test Mode 2.
3511 Status error after Header Write order. No abnormal status expected. See print-out.
3512 Controller not ready after Sense order in Test Mode 2.
3513 Header Write Tag Line error. Sense buffer: IOBF1. See print-out.
3514 Status error in diagnostic Sense byte (byte 8 of Sense data) defines Header Write error.
3515 Address received during Sense not expected. Head or Sector Address may not increment properly. See print-out.

TST1, 36 Test Mode 2 - 120 Sector Header Write Test. A Seek/CC/Header Write order sequence with a Header Write byte count of 960 is issued. A Sense order is issued to verify that the Head and Sector Address are incremented to Head 20 Sector 0.

3610 Controller not ready after Seek/CC/Header-Write orders in Test Mode 2.
3611 Byte count not zero after Header Write order (960 bytes).
3612 Status error after Header Write order. No abnormal status expected.
3613 Controller not ready after Sense order in Test Mode 2.
3614 Address received during Sense not expected. Header or Sector Address have not been incremented past Head 19 Sector 5.

TST1, 37 Test Mode 2 - Header Write Byte Count Test. Header Write orders with byte counts of 7 and 9 are issued to the controller and the Status Response is tested.

3710 Controller not ready after Seek/CC/Header-Write order in Test Mode 2.
3711 Status error after Header Write order (byte count 4). Expected: IL, no UE, byte count = 0. See print-out.
3712 See 3711. Header Write order byte count = 9.

TST1, 38 Test Mode 2 - Header Write Order Cylinder Boundary Test. A Header Write order with a byte count of 49 is issued starting at Head 19 Sector 0. Write operation will terminate after 6 sectors and sector unavailable will be reported.

3810 Controller not ready after Header Write order in Test Mode 2.
3811 Status error after Header Write order (Seek Address = Head 19, Sector 0, byte count = 49). UE, sector unavailable, byte count = 0 expected.

TST1, 39 Test Mode 2 - Header Write Starting Address Test. Header Write orders with Starting Sector Address of 0 through 5 are sequentially issued. For all Starting Addresses except 0, byte 8 of the Sense data will indicate Header Address error.

3910 Controller not ready after Header Write order in Test Mode 2.
3911 Status error after Header Write order. No abnormal status expected.
3912 Controller not ready after Sense order in Test Mode 2.
3920-3925 Status error in diagnostic Sense byte (byte 8 of Sense data). The least significant digit of error number reflects the Starting Sector Address of the Header-Write operation. Header-Address error is expected for all Starting Address except Sector 0.

TST1, 40 Test Mode 2 - Write Order Test. Seek/CC/Write order sequences are issued with Write byte count 3 or 1024. The Write data consists of byte values starting at 224, with each successive byte = byte (N) + 1. These values reflect the byte counter in the controller at the time of writing each byte. Status and byte count are verified. A Sense order verifies that the Tag Lines are correctly generated and that the Head and Sector Address increment correctly.

4010 Controller not ready after Seek/CC/Write orders in Test Mode 2.
4011 Status error after Write order. No abnormal status expected.
4012 Controller not ready after Sense order in Test Mode 2.
4013 Write Tag Line error. Sense buffer: IOBF1. See print-out.
4014 Status error in diagnostic Sense byte (byte 8 of Sense data) defines Write error.
4015 Address received during Sense not expected. Head and Sector Address may not increment properly. See print-out.

TST1, 41 Test Mode 2 - Write Order Incorrect Length Test. Seek/CC/Write order sequences are issued with byte counts sequentially varied from 1008 to 1025 (not 1024). The status will be verified.

4110 Controller not ready after Write order in Test Mode 2.
4111 Remaining byte count after Write order with Incorrect Length not zero. See print-out.
4112 Status error after Write order in Test Mode 2. IL expected. See print-out.

TST1, 42 Test Mode 2 - Write Order Cylinder Boundary Test. A Write order with a byte count of 1025 is issued starting at Head 19 Sector 5. The Write operation will terminate after 1 sector and sector unavailable will be reported.

4210 Controller not ready after Write order in Test Mode 2.
4211 Status error after Write order (Seek Address = Head 19, Sector 5 byte count 1025). UE, sector unavailable, byte count = 0 expected.

TST1, 45 Test Mode 2 - Check-Write Order Test. Seek/CC/Check-Write order sequences are issued with byte counts of 1024. The Check Write data consists of byte values starting at 224, with each successive byte = byte (N) +1. A Sense order verifies that the Tag Lines are correctly generated and that the Head and Sector Address increments correctly.

4510 Controller not ready after Seek/CC/Check-Write orders in Test Mode 2.
4511 Status error after Check-Write order. No abnormal status expected. See print-outs.
4512 Controller not ready after Sense order in Test Mode 2.
4513 Check-Write Tag Line error. Sense buffer: IOBF1. See print-out.
4514 Status error in diagnostic Sense byte (byte 8 of Sense data) defines Check-Write error.
4515 Address received during Sense not correct. Head or Sector Address may not increment properly. See print-out.

TST1, 46 Test Mode 2 - Check-Write Order Incorrect Length Test. Seek/CC/Check-Write order sequences are issued with byte counts sequentially varied from 1008 to 1025 (not 1024). The status will be verified.

4610 Controller not ready after Seek/CC/Check-Write order in Test Mode 2.
4611 Remaining byte count after Check-Write order with Incorrect Length not zero. See print-out.
4612 Status error after Check-Write order in Test Mode 2. IL expected. See print-out.

TST1, 47 Test Mode 2 - Check-Write Order Cylinder Boundary Test. A Check-Write order with a byte count of 1025 is issued starting at Head 19 Sector 5. The Check-Write operation will terminate after one sector and sector unavailable will be reported.

4710 Controller not ready after Check-Write order in Test Mode 2.
4711 Status error after Check-Write order (Seek address = Head 19, Sector 5, byte count 1025). UE, sector unavailable, byte count = 0 expected.

TST1, 48 Test Mode 2 - Check-Write Transmission Error Test. Seek/CC/Check-Write order sequences with byte counts of 2048 are issued. The Check-Write data consists of byte values starting at 224 (X'E0'), with each successive byte = byte (N) + 1. During the first 8 passes one bit in byte 32 (X'FF') is sequentially dropped starting with bit 0 ending with bit 7. During the 2nd 8 passes one bit in byte 33 (X'00') is sequentially picked-up starting with bit 0, ending with bit 7. The test verifies that a single bit failure in a sector is detected and reported as TE and that the operation terminates after the first sector. The remaining byte count must be ≥ 1000.

4810 Controller not ready after Seek/CC/Check-Write order in Test Mode 2.
4811 Remaining byte count after Check-Write order (2048 bytes) less than 1008. Check-Write operation did not terminate after one sector.
4812 Controller not ready after Sense order in Test Mode 2.
4813 Address received during Sense not correct. Head or Sector Address may have been incremented by two sectors.
4814 Status error in diagnostic Sense byte (byte 8 of Sense data) should indicate Check-Write error.
4820–4827 Status error after Check-Write order. TE and not IL or UE expected. The least significant digit of the error number indicates which bit of byte 32 of the Check-Write data was dropped to induce a Check-Write error.
4830–4837 See 4820–4827. The least significant digit of the error number indicates which bit of byte 33 of the Check-Write data was added to induce a Check-Write error.

TST1, 49 Test Mode 2 - Halt On Transmission Error Test. Seek/CC/Write order sequences with byte counts of 1020 are issued to test setting of UE, IL and IOP/Halt. Seek/CC/Check-Write order is issued to check setting of TE.

4910 Controller not ready after Seek/CC/Write (or Check-Write) in Test Mode 2.
4911 Status error after Write order in Test Mode 2. UE, IL and IOP/Halt setting expected.
4912 Status error after Write order in Test Mode 2. IL and not UE and not IOP/Halt setting expected.
4913 Status error after Check-Write order in Test Mode 2. UE, TE and IOP/Halt setting expected.

TST1, 50 Test Mode 3 (Parity) - Read Order 12 Parity Test. A Sense/CC/Read 12 order sequence is issued with a Read byte count of 2048. The controller will generate a parity error. The test verifies the status (TE and not UE) and verifies with a Sense order that the Read order terminated after a sector. The remaining byte count must be = 1024.

5010 Controller not ready after Seek/CC/Read 12 order in Parity Test Mode.
5011 Remaining byte count after Read 12 order (2048 bytes) not equal to 1024. Read 12 operation did not terminate after one sector.
5012 Status error after Read 12 order. TE and not IL or UE expected. See Print-out.
5013 Controller not ready after Sense order in Parity Test Mode.
5014 Status error in diagnostic Sense byte (byte 8 of Sense data) should indicate data parity error.
5015 Address received during Sense not correct. Head or Sector Address may have been incremented by 2 sectors.

TST1, 51 Test Mode 3 (Parity) - Read Order 02 Parity Test. A Sense/CC/Read 02 order sequence is issued with a Read byte count of 3072 (3 data-chain operation). The test verifies that Reading continues until the byte count = zero. The expected status is TE, not UE.

5110 Controller not reddy after Seek/CC/Read02/DC/Read02/DC/Read02 in Parity Test Mode.
5111 Status error after Read02 order. TE and not IL or UE and byte = zero and Current Command Address = Starting Address + 3 expected.
5112 Controller not ready after Sense order in Parity Test Mode.
5113 Address received during Sense not correct. Head or Sector Address did not increment correctly.

TST1, 52 Normal Mode - Restore Order Test. A Restore order is issued to the storage unit. The test verifies that the controller and device are ready and that positioning is complete and that no time out error has occurred.

5210 Controlled not ready after Restore order.
5211 On cylinder bit TDV(5) not received after Restore order.
5212 Status error after Device order. See print-out.

TST1, 53 Normal Mode - Seek Order Test. A Restore order is issued to the storage unit. The test proceeds to issue Seek orders for all sectors on cylinder 0. No head motion is involved except possibly during the Restore order. The test verifies that Seek orders can be completed without errors.

5310 Controller not ready after Seek order.
5311 On-cylinder bit TDV(5) not received after Seek order. No head motion required.
5312 Status error after Seek order. See print-out.

TST1, 54 Normal Mode - Release Order Test. A Release order is issued. The test verifies the status after the release.

5410 Controller not ready after Restore order in normal mode.
5411 Status error after Restore order in normal mode. Not UE, byte count = 1 (no change) expected. See print-out.

TST1, 55 Header Read - Failure Isolation Test. A Restore order is issued to position the heads at cylinder 0. Seek/CC/Header-Read sequences will be issued for all 120 sectors of cylinder 0. No errors will be reported until all operations are completed. A summary of all errors will be printed. The test will proceed to loop on the first failure with immediate error print-outs. Information other than zeros in the flaw byte or alternate Address byte will not be considered an error.

5510 Controller not ready after Seek/CC/Header Read order.
5511 Status error after Header-Read order. See print-out.
5512 Compare error of Header data. Bytes 0, 5 and 6 of each Header are not tested.

TST1, 56 Normal Mode - Sense Order/Angular Position. A Restore order is issued to the storage unit. The test issues a Sense order and verifies the status. The test proceeds to issue up to 6 Sense orders in order to verify angular position 0. Following position 0, 5 Sense orders are issued to verify angular position 1-5.

5610 Controller not ready after Sense order.
5611 Status error after Sense order. See print-out.
5612 Controller not ready after Sense order.
5613 6 attempts failed to find angular position of 0 in byte 4 of Sense data.
5621-5625 Controller not ready after Sense order. The least significant digit of the error number indicates the current angular position expected in the Sense data.
5631-5635 The expected angular position as indicated by the least significant digit of the error number not in byte 4 of Sense data.

TST1, 57 Normal Mode - Sense Order Test. A Restore order is issued to position the heads at cylinder 0. Seek/CC/Sense sequences will be issued for all 120 sectors of cylinder 0. The test verifies that the Address returned during the Sense operation is correct and that normal status is returned.

5710 Controller not ready after Sense order.
5711 Status error after Sense order. See print-out.
5712 Compare error of Seek and Sense data. See print-out.
5713 Status error in diagnostic Sense byte (byte 8 of Sense data) should indicate no errors.

TST1, 58 Sequential Head Positioning Test. Sequential Seek orders are issued to the disk storage unit. After verifying successful completion of each Seek order, a Sense order is issued to verify the Seek operation. If a Header parity error is detected during the Sense order, the Sense operation will be automatically retried six additional times before an error is reported. If the cylinder Address obtained is correct, the next Seek/Sense sequence will be initiated. On retries after a cylinder compare error, the Seek Address will be decremented by 1 (not < 0) and a Restore order will be issued prior to retry.

5810 Controller not ready after a Seek order.
5811 Controller not ready after Sense order. Arm was in motion execution of Sense order.
5812 Arm in motion bit in byte 4 of Sense data not received.
5813 On cylinder bit TDV(5) not received after Seek order. The Seek order intiated head motion.
5814 Controller not ready after Sense order. Arm motion was previously completed. TDV(5) = 1.
5815 All six Sense orders issued to the drive unit indicate that a Header parity error was detected.
5816 Compare error of Seek and Sense data. See print-out.

TST1, 60 Complex Head Positioning, Seek Access Timing and Seek Complete Interrupt Test. This test consists of four passes. The passes differ by the type of head motion.

1. Seek (M) Sense Seek (N) Sense 203 times. M varies from 0 to 202, N is always = 0.
2. Seek (M) Sense Seek (N) Sense 203 times. M is always 202. N varies from 202 to 0.
3. Seek (M) Sense Seek (N) Sense 203 times. M varies from 0 to 202, N varies from 202 to 0.
4. Seek (R) Sense Seek (R) Sense 203 times. R is a random number.

During retries the last successful Seek/Sense sequence is repeated. Average Seek access time is computed and if it exceeds the limit, it is printed out. The test is initialized if retry is requested.

6010 Controller not ready after Seek order.
6011 Expected Seek complete interrupt was not received.
6012 Status error after Seek complete interrupt has been received. See print-out.
6013 Controller not ready after Sense order.
6014 Header parity error indicated by bit 7 of TDV following Sense orders. The Sense order has been issued 7 times to automatically recover from the problem. Possible bad Headers on the disk.
6015 Head positioning error. See preceding print-out. The expected Sense data defines the Seek Address. The observed Sense data defines the Current Address in the controller. Prior to the Seek operation.
6016 Average Head positioning time greater than 95 msec. All Seek operations in this test are used in the computation of the average time.

TST1, 63 Comprehensive Write/Read/Checkwrite Test. During the first phase of this test, attempts are made to locate a cylinder with error-free Headers. The cylinders used are determined by the SYST-directive entry for each device. Once a good cylinder has been located, a Write/Read/Checkwrite pass will be performed 3 times, each time with a different pattern.
Pass 1: Fixed pattern of X'AA55AA55'
Pass 2: Incremented pattern of X'00010203', X'04050607', X'08090A0B'

TST1, 63 (Continued)

Pass 3: Current Seek Address X'00000000' for cyl = 0, HD=0, Sect=0, X'00NNN0803' for cyl=NN,HD=08,Sect=3. Any recoverable error (6 retries are automatically attempted) or solid failure will cause the selection of another cylinder. The objective of this procedure is to avoid looping on an error which may be caused by surface flaws.

6310 Attempts to find a cylinder (120 sectors) with good Headers and no assigned Alternate Addresses not successful. Program used only those cylinders which were made available to the program with the SYST directive.
6311 Controller not ready after Header Read order of 120 sectors.
6312 Byte count after Header Read order not reduced to zero.
6313 Status error after Header Read order. No unusual status expected.
6314 Header data compare error. See print-out. If a flaw byte or an Alternate Address is found in the Header, the current cylinder will not be used for the Write/Read/Checkwrite portion of this test.
6315 Header Read operation not successful for current cylinder. Errors 6311 through 6314 describe the nature of the failure. Next cylinder will be automatically selected.
6320 Controller not ready after Seek order.
6321 Controller not ready after Sense order.
6322 Seek/Sense compare error. See expected and observed data. The Sense order was issued after a Write, Read, or Checkwrite order. The Sense data should reflect the current Address.
6330 Controller not ready after Write order. Preceding Seek order successful.
6331 Status error after Write order. No unusual status expected. The Write order will be automatically retried 6 times.
6332 Status error after Write order. The diagnostic Sense byte (byte 8 of Sense data) should indicate no errors.
6333-6335 See 6330 through 6332, respectively. Current order was a Read. The sector in error may have been incorrectly written.
6336 Read compare error. See print-out. The error may result from incorrect writing of the data.
6337-6339 See 6330 through 6332, respectively. Current order was a Checkwrite. The sector in error may have been incorrectly written if Read errors are detected.
6340 Write errors on current cylinder. If Sense Switch 1 is reset and 3 set, the Read and Check-Write portion of this test will be skipped and a new cylinder will be selected. Fixed pattern of X'AA55AA55AA5...'.
6341 Read erros on current cylinder. If Sense Switch 1 is off and 3 on, the Checkwrite portion of this test will be skipped and a new cylinder will be selected. Fixed pattern of X'AA55AA55AA5...'.
6342 Checkwrite errors on current cylinder. If Sense Switch 1 is off and 3 on, a new cylinder will be selected. Fixed pattern of X'AA55AA55AA5...'.
6343 See 6340. Write errors. Incremented pattern X'00010203040506..'
6344 See 6341. Read errors. Incremented pattern X'00010203040506..'
6345 See 6342. Check-Write errors. Incremented pattern X'00010203040506...'.
6346 See 6340. Write errors. Current Seek Address used as pattern.
6347 See 6341. Read errors. Current Seek Address used as pattern.
6348 See 6342. Check-Write errors. Current Seek Address used as pattern.

TST1, 64 Short Record Write Test. During the first phase of this test, attempts are made to locate a sector which can be recorded and verified. Once a good sector has been located, a 4 byte record is written and verified with a Read order. Bytes 4 through 1023 are expected to be zero.

6410 Controller not ready after Seek/CC/Write order.
6411 Status error after Write order. Normal termination expected.
6412 Controller not ready after Seek/CC/Read order.
6413 Status error after Read order. Normal termination expected.
6414 Data compare error on current sector.
6415 Controller not ready after Seek/CC/Write order (4 bytes). The remaining bytes of the current sector should contain zeros.
6416 Status error after Write order (4 bytes). Only IL is expected.
6417 Controller not ready after Seek/CC/Read order (1024 bytes). The preceding Write order recorded only 4 bytes of data.
6418 Status error after Read order. Normal termination expected.
6419 Data compare error on current sector. If word count of compare error MSG > 0, the controller failed to write zeros for bytes 4 through 1023.
6420 Write or Read errors on current sector. Another sector, if available, will be selected.
6430 Device not ready after Seek/CC/Read (BC=253)/CC/Sense.
6431 Status error after Seek/CC/Read(BC=253)/CC/Sense. Normal termination expected.
6432 Device failed to report correct sector on sense at least once in 256 cycles of: Seek/CC/Read(BC=253)/CC/Sense.

TST1, 65 Header Write Test. This test will only be executed if cylinder 202 is made available to the test program with the SYST directive. The test will write all Headers on cylinder 202 for Heads 16 through 19. The original Headers will be saved at the start of the test and restored at the end of the test.

6510 Controller not ready after Seek/CC/Header Write order (6 sectors).
6511 Status error after Header Write order. Normal termination expected.
6512 Controller not ready after Seek/CC/Header Read order (6 sectors).
6513 Status error after Header Read order. Normal termination expected. Headers may have been incorrectly written.
6514 Header compare errors. Each Header consists of 8 bytes. Headers may have been incorrectly written.
6515 Controller not ready after Sense order.
6516 Status in diagnostic Sense byte (byte 8 Sense data) should indicate no errors.
6517 Attempts to save 24 Headers starting at cylinder 202, Head 16, Sector 0 not successful. Remainder of this test will be skipped.

TST1, 66 Header Error Detection Test. This test will only be executed if cylinder 202 is made available to the test program with the SYST directive. The test consists of the following 3 sections:

1. Headers with flaw bytes are written for cylinder 202, Head 17 Sense, Header Read, and Read orders are issued to verify the detection of the flaw byte and setting of UE (UE will not be set during Header Read).
2. Headers with a cylinder address of 225 are written for cylinder 202, Head 18. A Sense order is issued to verify the setting of verification error, UE, and cylinder compare error (byte 8 of Sense data).
3. Headers for cylinder 202, Head 19 contain the following information: Sector 0 OK, Sector 1 OK, Sector 2 OK, Sector 3 cylinder wrong, Sector 4 Head wrong, Sector 5 sector wrong.
4. Header Read and Read orders are issued to verify that cylinder, head, and sector compare errors are set (byte 8 of Sense data) and that the orders terminate correctly after detection of an erroneous Header.

The original Headers will be saved at the start of the test and restored at the end of the test.

6610 See 6517
6611 Controller not ready after Seek/CC/Header Write order (24 sectors).
6612 Status error after Header Write order. Normal termination expected.
6620 Controller not ready after Seek/CC/Sense order. All six headers starting at cylinder 202, Head 17 have flaw bytes recorded from preceding Write Pass.
6621 Status error after Sense order. UE, flaw byte (TDV bit 1) and not TE expected. All six headers starting at cylinder 202, Head 17 have flaw bytes recorded from preceding Write Pass.
6622 Controller not ready after Seek/CC/Header Read order. See also 6620.
6623 Status error after Header Read order. Flaw byte, not UE or TE expected. See also 6621.
6624 Controller not ready after Seek/CC/Read order. See also 6620.